Remarks

Rejections Under 35 U.S.C. § 102(b)

The Examiner has rejected claims 1-6 and 10-11 under 35 U.S.C. § 102(b) as anticipated by United States patent number 6,032,214 issued to Farmwald et al, hereinafter referred to as Farmwald. The Applicants have canceled claims 1 and 10 and amended claims 2 and claim 11 to overcome the Examiner's rejections to these claims under 35 U.S.C. § 102(b). Because claim 1 and claim 10 have been canceled, the Applicants respectfully request withdrawal of the rejections of these claims under 35 U.S.C. § 102(b).

The amended claim 2 includes the limitations of "storing the first value in a storage device, with the first value including a plurality of bits and ***with those of the plurality of bits in a first state corresponding to clock cycles during which the usage of the bus occurs for the transaction***". (emphasis added) The amended claim 11 includes the limitations of "a second value including a first plurality of bits, with positions ***within the second value of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus***". (emphasis added).

The Applicants respectfully contend that Farmwald does not teach or suggest these limitations of the amended claim 2 and the amended claim 11. On page 2 of the office action, in making the rejections of claims 1-6 and 10-11, the Examiner has relied upon the subject matter disclosed in column 6, line 52 through column 7, line 5 of Farmwald, column 9, lines 21-36 of Farmwald, and column 12, line 56 through column 13, line 3 of Farmwald.

For example, column 9, lines 21-36 of Farmwald discloses, among other things, a "request packet 22" and discloses that "[s]etting 23 AddrValid=1 in an otherwise unused cycle indicates the start of an request packet (control information)". And, column 12, line 56 through column 13, line 3 of Farmwald discloses, among other things, " [a] simple method is for each master to maintain a bus-busy data structure, for example by maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be free, that is, the end of the latest pending data block transfer." The Applicants respectfully contend that nowhere in these cited sections of Farmwald are there teachings upon which the limitations from the amended claim 2 or limitations from the amended claim 11

can read. The Applicants can discern no teaching of "***those of the plurality of bits in a first state corresponding to clock cycles during which the usage of the bus occurs***" (from the amended claim 2) or "***with positions within the second value of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus***" (from the amended claim 11) in Farmwald. Where is the teaching in Farmwald that discloses these limitations? If the Examiner asserts such teaching is present within Farmwald, the Applicants respectfully request that this teaching is specifically identified and the Examiner's asserted correspondence between the terms of the cited sections of the amended claim 2 and the amended claim 11 and the teachings in Farmwald is explained.

According to MPEP section 2131, "A claim is anticipated only if ***each and every element*** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (emphasis added) Because, according to MPEP section 2131 cited above, the sections of Farmwald cited by the Examiner do not teach or suggest "each and every element" as set forth in the amended claim 2 and the amended claim 11, the amended claim 2 and the amended claim 11 are not anticipated under 35 U.S.C. § 102(b) for at least this reason. Accordingly, the Applicants respectfully request withdrawal of the rejections of the amended claim 2 and the amended claim 11 under 35 U.S.C. § 102(b) based upon Farmwald.

Claims 3-6 are dependent upon claim 1, either directly or indirectly, and therefore incorporate by reference all the limitations of claim 1 and so are not anticipated by Farmwald for at least this reason. Therefore, the Applicants respectfully request withdrawal of the rejections of claims 3-6 under 35 U.S.C. § 102(b) based upon Farmwald.

Rejections of Claims 7-9, and 12 Under 35 U.S.C. § 103(a)

The Examiner has rejected claims 7-9 and 12 under 35 U.S.C. § 103(a) as obvious in view of Farmwald over United States Patent number 5,581,782, issued to Sarangdhar et al (hereinafter referred to as Sarangdhar). According to MPEP 2143, one element that must be met to make a valid prima facie obviousness rejection is that "the prior art reference (or references when combined) must teach or suggest ***all the claim limitations.***" (emphasis added) Claims 7-9 depend indirectly upon the amended claim 2

and therefore incorporate all the limitations of the amended claim 2. Because Farmwald does not teach or suggest all the limitations of the amended claim 2 as explained above and the cited sections of Sarangdhar do not teach or suggest these limitations, a valid prima facie obviousness rejection of claims 7-9 has not been established for at least this reason. Accordingly, the Applicants respectfully request withdrawal of the rejections of claims 7-9 under 35 U.S.C. § 103(a).

Claim 12 depends indirectly upon the amended claim 11 and therefore incorporates all of the limitations of the amended claim 11. Because Farmwald does not teach or suggest all the limitations of the amended claim 11, a valid prima facie obviousness rejection of claim 12 has not been established for at least this reason. Accordingly, the Applicants respectfully request withdrawal of the rejection of claim 12 under 35 U.S.C. § 103(a).

Rejections of Claims 22-31 Under 35 U.S.C. § 103(a)

The Examiner has rejected claims 22-34 under 35 U.S.C. § 103(a) as obvious in view of Farmwald over Sarangdhar. Claim 22 includes the limitations of "setting a first plurality of bits to a level, with ***each of the first plurality of bits set to the level indicating the usage of the bus during a corresponding one of a first plurality clock cycles*** to occur". (emphasis added) The Applicants respectfully contend that neither Farmwald or Sarangdhar disclose these limitations. The sections of Farmwald relied upon by the Examiner have been discussed at length previously. If the Examiner asserts such teaching is present within Farmwald, the Applicants respectfully request that this teaching is specifically identified and the Examiner's asserted correspondence between the terms of the cited sections of claim 22 and the teachings in Farmwald is explained.

The section of Sarangdhar cited states, among other things, that "[a]nother element that may be included is an ownership state indicator that indicates the ownership state of the system bus. If the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle earlier than if the ownership state is a second state." There is no teaching here of the limitations of claim 22 previously recited in this paragraph in this section of Saragdhar. If the Examiner asserts such teaching is present within the cited section of Saragdhar, the Applicants respectfully request that this teaching is specifically identified and the Examiner's asserted

correspondence between the terms of the cited sections of claim 22 and the teachings in Saragdhar is explained. Because neither Farmwald or Saragdhar alone of in combination teach or suggest all the limitations of claim 22, claim 22 is not obvious over these references for at least this reason. Furthermore, claims 23-31 which incorporate by reference the limitations of claim 22, are not obvious over these references for at least this reason. Accordingly, the Applicants respectfully request withdrawal of the rejections of claims 22-31 under 35 U.S.C. § 103(a).

Rejections of Claims 32-34 Under 35 U.S.C. § 103(a)

The Examiner has rejected claims 32-34 under 35 U.S.C. § 103(a) as obvious in view of Farmwald over Sarangdhar. Claim 32 includes the limitations ofthose of the plurality of ***bits at a first level indicating usage of a bus during a first set of corresponding clock cycles*** and with those of the plurality of ***bits at a second level indicating no usage of the bus during a second set of corresponding clock cycles***". (emphasis added) The Applicants contend that the sections of Farmwald and Saragdhar cited by the Examiner do not teach or suggest the above cited limitations of claim 32. If the Examiner asserts such teaching is present within the cited section of Saragdhar or Farmwald, the Applicants respectfully request that this teaching is specifically identified and the Examiner's asserted correspondence between the terms of the cited sections of claim 32 and the teachings in Saragdhar or Farmwald is explained.

Objections to the Claims

The Examiner has objected to claims 13-15 as containing allowable subject matter but dependent upon a rejected base claims. The Applicants respectfully request that the objections to claims 13-15 be held in abeyance until a decision is made on the allowability of the rejected claims upon which these claims depend.

Allowable Subject Matter

The Examiner has indicated that claims 16-21 are allowed.

Conclusion

The Applicants respectfully contend that the subject application is in a condition for allowance. Allowance is respectfully requested.

Respectfully submitted,
John R. McVey, et al.

By Gregg W. Wisdom
Gregg W. Wisdom
Reg. No. 40,231

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(360) 212-8052